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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,243	11/13/2003	Bomy Chen	2102397-992740	2456

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,243	CHEN ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,8-11 and 14-24* is/are pending in the application.

4a) Of the above claim(s) *20-24* is/are withdrawn from consideration.

5)☒ Claim(s) *5,8-11,14 and 15* is/are allowed.

6)☒ Claim(s) *1,4 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1105*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 11/25/2005.

Claims 1, 4, 5, 8-11, and 14-24 are active in this application, in which claims 20-24 have been withdrawn.

Claim(s) 2, 3, 6, 7, 12, and 13 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 11/14/2005. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Remarks

3. Applicant's argument(s) filed 11/25/2005 have been considered, but are moot in view of new ground of rejection(s).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 16 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,151,248 to Harari et al., or by U.S. Patent No. 6,316,315 to Hofmann et al.

Regarding claim 16, Harari discloses a NAND circuit device, as shown in figs. 3-7, comprising:

a plurality of stacked gate non-volatile memory cells arranged in a plurality of rows and columns; each cell having a first terminal 49 and second terminal 51 with a channel region therebetween, a floating gate 56/57 spaced apart and insulated from said channel region, a control gate 99 capacitively coupled with said floating gate 56/57, and a tunnel material between said floating gate and said control gate configured to permit Fowler-Nordheim tunneling of charges from said floating gate to said control gate to effect erasure (see col. 8, lines 52-62);

wherein said cells in the same row are connected with each cell having a common second terminal 51 with an adjacent cell to one side, and having a common first terminal 49 with an adjacent cell to another side;

wherein cells in the same row have the control gate 99 connected together (through line 92-94); and wherein cells in adjacent rows are separated by isolation (isolating material between adjacent cells to isolate one cell from another).

Similarly, Hofmann discloses a NAND circuit device, as shown in figs. 1-10, comprising:

a plurality of stacked gate non-volatile memory cells arranged in a plurality of rows and columns; each cell having a first terminal 45 and second terminal 60 with a channel region 25 therebetween, a floating gate 40 spaced apart and insulated from said channel region 25 (by gate dielectric 30), a control gate 120/140 capacitively coupled with said floating gate 40, and a tunnel material 110/115 between said floating gate 40 and said control gate 120/140 configured to permit Fowler-Nordheim tunneling of charges from said floating gate to said control gate to effect erasure (see col. 7, lines 43-48;

wherein said cells in the same row are connected with each cell having a common second terminal 60 with an adjacent cell to one side, and having a common first terminal 45 with an adjacent cell to another side;

wherein cells in the same row have the control gate 120/140 connected together (through line 130); and wherein cells in adjacent rows are separated by isolation (isolating material between adjacent cells to isolate one cell from another).

6. Claim(s) 1, 4, and 16-19 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,541,815 to Mandelman et al.

Regarding claim 1, Mandelman discloses a non-volatile memory cell, as shown in figs. 1-17, comprising:

a substantially single crystalline substrate 10 of a first conductivity type having a planar surface;

a trench 16 in said planar surface, said trench having a side wall and a bottom;

a floating gate FG1A/FG1B in said trench spaced apart and insulated from said sidewall and from said bottom; said floating gate having a tip away from said bottom;

a first region S0/S1 of a second conductivity type in said bottom;

a second region D1/D2 of a second conductivity type along said planar surface, spaced apart from said first region;

a channel region between said first region and said second region, said channel region along said sidewall;

a control gate C0-C3 capacitively coupled to said floating gate and capable of effecting erase; and

a tunnel material between said tip and said control gate, wherein said tunnel material is a tunnel oxide and configured to permit Fowler-Nordheim tunneling of charges from said floating gate to said control gate. See col. 4, lines 25-35.

Regarding claim 4, Mandelman discloses the he memory cell further comprising an insulation material between said floating gate and said sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said floating gate. See col. 1, lines 33-42; col. 4, lines 40-51.

Regarding claim 16, Mandelman discloses a NAND circuit device, as shown in figs. 1-17, comprising:

a plurality of stacked gate non-volatile memory cells arranged in a plurality of rows and columns; each cell having a first terminal S1 and second terminal D1 with a channel region therebetween, a floating gate FG1A/FG1B spaced apart and insulated from said channel region, a control gate C1 capacitively coupled with said floating gate, and a tunnel material between said floating gate FG1 and said control gate C1 configured to permit Fowler-Nordheim tunneling of charges from said floating gate to said control gate to effect erasure (see col. 4, lines 25-35);

wherein said cells in the same row are connected with each cell having a common second terminal D1 with an adjacent cell to one side, and having a common first terminal S1 with an adjacent cell to another side;

wherein cells in the same row have the control gate connected together; and

wherein cells in adjacent rows are separated by isolation.

Regarding claim 17, Mandelman discloses the device wherein said first terminal S1 is in a trench 16 and said second terminal D1 is not in a trench. See figs. 2-12.

Regarding claim 18, Mandelman discloses the device wherein said floating gate of cells in the same row are capacitively coupled to the same control gate. See figs. 1-2.

Regarding claim 19, Mandelman discloses the device wherein cells in the same column have the same first terminal and the same second terminal. See figs. 1-17.

Allowabilites

7. Claims 5, 8-11, 14 and 15 are in condition for allowance.

The following is an examiner's statement of reasons for allowance:

None of the references of record teaches or suggests the claimed array of non-volatile memory cells comprising (in addition to the other limitations in the claim) a contact in a trench electrically connected to the first region of a first section and electrically connected to the first region of a second section of the first trench (claim 5); or

None of the references of record teaches or suggests the claimed array of non-volatile memory cells wherein a first cell in a first row includes a first contact in the trench electrically connected to the first region of the first cell and wherein the first contact is electrically connected to the first region of a second cell in a second row separated from the first row by at least one isolation row (claim 10).

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
February 14, 2006